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EXAMINER	
LEE, CHRISTOPHER E	
ART UNIT	**PAPER NUMBER**
2112	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/681,446	KOBAYASHI ET AL.	
	Examiner	Art Unit	
	Christopher E. Lee	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-61* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33,35-38,40-42,45-51 and 54-61* is/are rejected.

7)☒ Claim(s) *34,39,43,44,52 and 53* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 October 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/3/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Receipt Acknowledgement

1. Receipt is acknowledged of the Amendment filed on 3rd of March 2006. Claims 26, 40, 41, and 54 have been amended; no claim has been canceled; and no claim has been newly added since the Non-Final Office Action was mailed on 28th of November 2005. Currently, claims 1-61 are pending in this Application.

Specification

2. The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicants' use.

Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

(a) TITLE OF THE INVENTION.
(b) CROSS-REFERENCE TO RELATED APPLICATIONS.
(c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.
(d) THE NAMES OF THE PARTIES TO A JOINT RESEARCH AGREEMENT
(e) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC (See 37 CFR 1.52(e)(5) and MPEP 608.05. Computer program listings (37 CFR 1.96(c)), "Sequence Listings" (37 CFR 1.821(c)), and tables having more than 50 pages of text are permitted to be submitted on compact discs.) or
REFERENCE TO A "MICROFICHE APPENDIX" (See MPEP § 608.05(a). "Microfiche Appendices" were accepted by the Office until March 1, 2001.)
(f) BACKGROUND OF THE INVENTION.
(1) Field of the Invention.
(2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.
(g) BRIEF SUMMARY OF THE INVENTION.
(h) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).
(i) DETAILED DESCRIPTION OF THE INVENTION.
(j) CLAIM OR CLAIMS (commencing on a separate sheet).
(k) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).
(l) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

In this case, the specification does not arrange BRIEF SUMMARY OF THE INVENTION before BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS on page 4.

3. The disclosure is objected to because of the following informalities:

Substitute "signal" by --single-- in line 7 on paragraph [0023].

Appropriate correction is required.

Allowable Subject Matter

4. The indicated allowability of claims 1-61 are withdrawn in view of the newly discovered reference(s) to Dale [GB 2 382 180; cited by the Applicants], Nalawadi et al. [US 2003/0009654 A1; hereinafter Nalawadi], Rankin et al. [US 5,613,071 A; hereinafter Rankin], Shimada et al. [US 6,237,120 B1; hereinafter Shimada]. Rejections based on the newly cited reference(s) follow.

Drawings

5. The drawings are objected to because:

In the Figure 9, Step 915 does not commensurate with the disclosure in the specification. In fact, the specification paragraph [0050] on page 17, lines 8-9 states "as shown in block 915, the target SMBase may be restored to targeting the first processor's SMBase address." However, the Step 915 shows "executing the first SMI handler using the second processor's SMBase as the target SMBase," which is exactly same as Step 910 in the Figure 9.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where

necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

6. Claims 31, 37, 38, 42, and 58 are objected to because of the following informalities:

The claim 31 recites the subject matters "the second SMI" in line 1, and "the first SMI handler" in lines 1-2 and 5. However, they have not been specifically clarified in the claim 31 and its intervening claims. Therefore, the Examiner presumes that the term "the second SMI" could be considered as --a second SMI--, and the term "the first SMI handler" could be considered as --the SMI handler-- in light of the specification since they are not defined in the claims, respectively.

The claim 37 recites the subject matter "the first SMBase address" in line 2. However, it has not been specifically clarified in the claim 37 and its intervening claims. Therefore, the Examiner presumes that the term "the first SMBase address" could be considered as --a first SMBase address-- in light of the specification since it is not defined in the claims.

The claim 38 recites the subject matters "the target SMBase" and "the SMI handler" in line 3. However, they have not been specifically clarified in the claim 38 and its intervening claims. Therefore, the Examiner presumes that the term "the target SMBase" could be considered as --a target SMBase--, and the term "the SMI handler " could be considered as --the SMI code-- in light of the specification since they are not defined in the claims, respectively.

The claim 42 recites the subject matters "the first memory address" in line 1. However, it has not been specifically clarified in the claim 42 and its intervening claims. Therefore, the Examiner presumes that the term "the first memory address" could be considered as --the first memory location-- in light of the specification since it is not defined in the claims.

The claim 58 recites the subject matters "the target SMBase" in line 1. However, it has not been specifically clarified in the claim 58 and its intervening claims. Therefore, the Examiner presumes that the term "the target SMBase" could be considered as --a target SMBase-- in light of the specification since it is not defined in the claims.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 2, 3, and 8-11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The claims 2, 3, 8, 9, and 11 recite a subject matter "the second processor", respectively. However, their prior claim 1 defines two different subject matters "a second processor" in lines 5 and 6. Therefore, the recalled subject matter "the second processor" in the claims 2, 3, 8, 9, and 11 fails to clearly point out which one of the two different subject matters "a second processor" in lines 5 and 6 of the claim 1, is the antecedent basis of the subject matter "the second processor" in the claims 2, 3, 8, 9, and 11, respectively, and then it makes the claims 2, 3, 8, 9, and 11 be indefinite. The Examiner presumes that the term "a second processor" in line 6 of the claim 1 could be considered as --the second processor-- in light of the specification since it is not clearly pointed out in the claims.

The claim 10 is a dependent claim of the claim 9.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

10. Claims 1, 3-5, 12-14, 18, 22, 23, 45, and 47-49 are rejected under 35 U.S.C. 102(a) as being anticipated by Dale [GB 2 382 180].

Referring to claim 1, Dale discloses a method (i.e., a method for waking up components in a dual-processor based system; See Abstract) comprising:

- receiving a first system management interrupt (SMI; i.e., initiating signal for waking up process; See Steps 405-415 in Fig. 4, in fact, RF_Module 340 receiving RF_RADIO_ON signal 370 in Fig. 3; See page 18, lines 6-11);
- handling the first SMI (i.e., said initiating signal for waking up process) with a first processor (i.e., GSM Processor 312 of Fig. 3; See page 20, lines 15-23);
- generating a wake-up signal (i.e., interrupt signal for waking up MMI Processor 322 of Fig. 3) with the first processor (in fact, said interrupt signal was caused by said RF_RADIO_ON signal from said GSM Processor; See page 18, lines 27-30);
- awakening a second processor (i.e., said MMI Processor), based on the wake-up signal (i.e., said interrupt signal) from the first processor (See page 18, lines 30-31); and
- handling the first SMI (i.e., said waking up process) with the second processor (See page 19, lines 1-4).

Referring to claim 3. Dale teaches

- the first and second processors (i.e., GSM 312 and MMI 322 Processors in Fig. 3) are physical processors (See page 12, lines 5-6, and 15).

Referring to claim 4. Dale teaches that handling the first SMI (i.e., said initiating signal for waking up process) with a first processor (i.e., GSM Processor 312 of Fig. 3; See page 20, lines 15-23) comprises:

- executing a default SMI handler (i.e., instructions being executed by said GSM Processor at Step 490 in Fig. 4) located at a first memory address (i.e., memory element having said instructions in Memory 350 in Fig. 3; See page 21, lines 9-14).

Referring to claim 5. Dale teaches the wake-up signal (i.e., interrupt signal for waking up MMI Processor 322 of Fig. 3) comprises

- a vector based (i.e., processor interrupt signal inherently anticipates the claimed subject matter "vector based") on the first memory address (i.e., interruption signal generated for said MMI Processor; See page 18, line 27 through page 19, line 4).

Referring to claim 12. Dale discloses a method (i.e., a method for waking up components in a dual-processor based system; See Abstract) comprising:

- receiving a first system management interrupt (SMI; i.e., initiating signal for waking up process; See Steps 405-415 in Fig. 4, in fact, RF_Module 340 receiving RF_RADIO_ON signal 370 in Fig. 3; See page 18, lines 6-11);

- executing code (i.e., waking up process) at a first memory address (i.e., Memory 350 of Fig. 3) with a first processor (i.e., GSM Sub-system 310 of Fig. 3) in response to the first SMI (See page 20, lines 15-23);
- generating a wake-up signal (i.e., interrupt signal for waking up MMI Processor 322 of Fig. 3) with the first processor (in fact, said interrupt signal was caused by said RF_RADIO_ON signal from said GSM Sub-system; See page 18, lines 27-30);
- awakening a second processor (i.e., MMI Sub-system 320 of Fig. 3), based on a wake-up signal (i.e., said interrupt signal) from the first processor (See page 18, lines 30-31); and
- executing the code (i.e., said waking up process) at the first memory address (i.e., said Memory) with the second processor (See page 19, lines 1-4).

Referring to claim 13, Dale teaches

- the wake-up signal (i.e., interrupt signal for waking up MMI Sub-system 320 in Fig. 3) is based on the first memory address (i.e., processor interrupt signal inherently anticipates that said interrupt wake-up signal is based on vector address in said Memory; See page 18, line 27 through page 19, line 4).

Referring to claim 14, Dale teaches

- the first memory address (i.e., Memory 350 of Fig. 3) is the location of default SMI handling code (i.e., instructions being executed by GSM Processor at Step 490 in Fig. 4 inherently anticipates that the first memory address is the location of default SMI handling code; in fact, memory element having said instructions in Memory 350 in Fig. 3; See page 21, lines 9-14).

Referring to claim 18, Dale teaches

- the first and second processors (i.e., GSM 310 and MMI 320 Sub-systems in Fig. 3) are physical processors (See page 12, lines 5-6, and 15) located on separate packages (i.e., said GSM Sub-system is packaged with GSM Processor 312, and said MMI Sub-system is packaged with MMI Processor 322 in Fig. 3; See page 12, lines 5-6, and 15).

Referring to claim 22. Dale teaches

- generating the SMI (i.e., GSM ULPD 314 of Fig. 3 generates the SMI, which is an initiating signal for waking up process; See Steps 405-415 in Fig. 4) before receiving the SMI with a first and second processor (in fact, RF_Module 340 receiving RF_RADIO_ON signal 370 before receiving the initiating signal for waking up process with the GSM Sub-system 310 and MMI Sub-system 320 in Fig. 3; See page 15, lines 4-10 and page 18, line 6 through page 19, line 11).

Referring to claim 23. Dale teaches generating the SMI (i.e., GSM ULPD 314 of Fig. 3 generates the SMI, which is an initiating signal for waking up process; See Steps 405-415 in Fig. 4) comprises

- changing the logic level (i.e., RF_RADIO_ON signal 370 being set in Fig. 3) of a pin (i.e., connection pin of GPIO 321 in Fig. 3) coupled to a controller hub (i.e., said GPIO; See page 16, line 28 through page 17, line 2).

Referring to claim 45. Dale discloses a system (i.e., cellular communication device in Fig.3) comprising:

- a controller hub (i.e., GSM ULPD 314 of Fig. 3) to generate a first system management interrupt (SMI; i.e., initiating signal for waking up process; See Steps 405-415 in Fig. 4, in fact, RF_Module 340 receiving RF_RADIO_ON signal 370 in Fig. 3; See page 18, lines 6-11);

- a memory (i.e., Memory 350 of Fig. 3) with a first memory address (i.e., memory element in said Memory) that contains code (i.e., waking up process; See page 20, lines 15-23);
- a first processor (i.e., GSM Processor 312 of Fig. 3) coupled to the controller hub (actually, said GSM Processor being coupled to said GSM ULPD in Fig. 3) to handle the first SMI (i.e., said waking up process), wherein
    - the first processor executes the code at the first memory address and generates a wake-up signal (in fact, said interrupt signal was caused by said RF_RADIO_ON signal from GSM Sub-system 310 in Fig. 3; See page 18, lines 27-30); and
- a second processor (i.e., MMI Processor 322 of Fig. 3) coupled to the controller hub (actually, said MMI Processor being coupled to said GSM ULPD via GPIO 321 in Fig. 3) to handle the first SMI (i.e., said waking up process) after receiving the wake-up signal (See page 16, line 28 through page 17, line 2), wherein
    - the second processor (i.e., said MMI Processor) executes the code at the first memory address (See page 18, lines 30-31 and page 19, lines 1-4).

Referring to claim 47, Dale teaches

- the first and second processors (i.e., GSM 312 and MMI 322 Processors in Fig. 3) are physical processors (See page 12, lines 5-6, and 15) located on separate packages (i.e., said GSM Processor 312 is packaged within GSM Sub-system 310, and said MMI Processor is packaged within MMI Sub-system 320 in Fig. 3; See page 12, lines 5-6, and 15).

Referring to claim 48, Dale teaches

- a pin (i.e., output pin from GSM ULPD 314 in Fig. 3) is toggled (i.e., RF_RADIO_ON signal 370 being set/reset in Fig. 3) on the controller hub (i.e., said GSM ULPD) to generated the first SMI

(i.e., GSM ULPD 314 of Fig. 3 generates the SMI, which is an initiating signal for waking up process; See Steps 405-415 in Fig. 4).

Referring to claim 49, Dale teaches

- code (i.e., Steps 405-415 in Fig. 4) is executed by the controller hub (i.e., GSM ULPD 314 of Fig. 3) to generate the first SMI (i.e., said GSM ULPD generates the SMI, which is an initiating signal for waking up process; See page 18, lines 6-14).

11. Claims 26-33, 35-38, 54-59, and 61 are rejected under 35 U.S.C. 102(b) as being anticipated by Nguyen et al. [US 2002/0099893 A1; hereinafter Nguyen].

Referring to claim 26, Nguyen discloses a method (i.e., method for handling of system management interrupts in a multiprocessor computer system; See Abstract) comprising:

- receiving an system management interrupt (i.e., all the processors receiving SMI; See paragraph [0017], lines 15-20);
- executing a SMI handler (e.g., Operating code for SMI handler of Processor 12c in Fig. 1) to handle a SMI (i.e., SMI issued by chipset; See step 46 in Fig. 2) for a first processor (i.e., Processor 12c of Fig. 1; in fact, said Operating code for SMI handler of Processor 12c could process said received SMI for said Processor 12c itself in Fig. 1; See paragraphs [0005] and [0018]); and
- executing the SMI handler (i.e., said Operating code for SMI handler of Processor 12c in Fig. 1) to handle the SMI (i.e., said SMI issued by chipset) for a second processor (e.g., Processor 12b of Fig. 1; in fact, said Operating code for SMI handler of Processor 12c could execute said received SMI for SMI initiating Processor 12b using parameters for said Processor 12b in Fig. 1; See

paragraph [0018]).

Referring to claim 27, Nguyen teaches

- the SMI (i.e., SMI issued by chipset; See step 46 in Fig. 2) is a software generated SMI (i.e., software SMI; See paragraph [0017], lines 21 through 27).

Referring to claim 28, Nguyen teaches

- the first processor (i.e., Processor 12c of Fig. 1) executes the SMI handler (i.e., Operating code for SMI handler of Processor 12c in Fig. 1) to handle the SMI (i.e., SMI issued by chipset; See step 46 in Fig. 2) for the first and the second processor (i.e., Processor 12c and Processor 12b in Fig. 1; See paragraphs [0005] and [0018]).

Referring to claim 29, Nguyen teaches

- the SMI handler (i.e., Operating code for SMI handler of Processor 12c in Fig. 1) is located at a first memory address (i.e., memory location for said Operating code; See paragraphs [0005] and [0019]).

Referring to claim 30, Nguyen teaches

- the first memory address (i.e., memory location for Operating code for SMI handler of Processor 12c in Fig. 1) is a default offset (i.e., a predetermined address at said memory location of said Operating code) from a first system management base (SMBase) address (i.e., a starting address of SMRAM space 84 in Fig. 3) for the first processor (i.e., said Processor 12c of Fig. 1, in fact, said Processor 12c is designated as default SMI handling processor, wherein said Operating code

is located at said predetermined address; See paragraphs [0005], [0008], and [0019]).

Referring to claim 31, Nguyen teaches handling a second SMI (i.e., SMI issued by chipset; See step 46 in Fig. 2) with the SMI handler (i.e., Operating code for SMI handler of Processor 12c in Fig. 1) comprises:

- changing a target SMBase of the SMI handler from the first SMBase (i.e., SMRAM space 84 in Fig. 3) to a second SMBase for the second processor (i.e., SMRAM space 82 of Fig. 3 for Processor 12b of Fig. 1); and
- executing the SMI handler using the second processor's SMBase as the target SMBase (See paragraphs [0018]-[0020]).

Referring to claim 32, Nguyen discloses a method (i.e., method for handling of system management interrupts in a multiprocessor computer system; See Abstract) comprising:

- executing system management interrupt (SMI) code (e.g., Operating code for SMI handler of Processor 12c in Fig. 1) with a first processor (i.e., said Processor 12c of Fig. 1) to handle a SMI (i.e., SMI issued by chipset initiated by peripheral devices, e.g., keyboard, etc.) for the first processor (in fact, said Operating code for SMI handler of Processor being executed for said initiating peripheral device; See paragraphs [0005] and [0006]);
- checking if the SMI is a software generated SMI (i.e., if the SMI issued by chipset initiated by a Processor; See step 46 in Fig. 2, in fact, software SMI; See paragraph [0017], lines 21 through 27; actually, checking SMI signature in SMRAM 78 of Fig. 3); and
- executing the SMI code (i.e., said Operating code for SMI handler) to handle the SMI for a second processor (i.e., Processor 12b of Fig. 1), if the SMI is software generated (See paragraph [0018], lines 13-28).

Referring to claim 33. Nguyen teaches

- the first processor (i.e., Processor 12c of Fig. 1) executes the SMI code (i.e., Operating code for SMI handler of said Processor 12c in Fig. 1) to handle the SMI for the second processor (i.e., SMI issued by chipset, which has been initiated by Processor 12b in Fig. 1; See steps 40-46 in Fig. 2), if the SMI is software generated (i.e., after checking SMI signature in SMRAM 78 of Fig. 3).

Referring to claim 35. Nguyen teaches

- the first processor (i.e., Processor 12c in Fig. 1) has a first system management base (SMBase) address (i.e.. address of SMRAM space 84 in Fig. 3).

Referring to claim 36. Nguyen teaches

- the second processor (i.e., Processor 12b in Fig. 1) has a second SMBase address (i.e., address of SMRAM space 82 in Fig. 3).

Referring to claim 37. Nguyen teaches

- said SMI code (i.e., Operating code for SMI handler of Processor 12c in Fig. 1) is located at first memory location (i.e., memory location for said Operating code), which has an offset (i.e., a predetermined address at said memory location of said Operating code) from a first SMBase address (i.e., from a starting address of SMRAM space 84 in Fig. 3; in fact, said Processor 12c is designated as default SMI handling processor, wherein said Operating code is located at said predetermined address; See paragraphs [0005], [0008], and [0019]).

Referring to claim 38. Nguyen teaches executing said SMI code (i.e., said Operating code for SMI handler) to handle the SMI for the second processor (See paragraph [0018], lines 13-28) comprises:

- changing a target SMBase of the SMI code from the first SMBase (i.e., SMRAM space 84 in Fig. 3) to the second SMBase (i.e., SMRAM space 82 of Fig. 3 for Processor 12b of Fig. 1); and
- executing the SMI code using the second processor's SMBase as the target SMBase (See paragraphs [0018]-[0020]).

Referring to claim 54. Nguyen discloses an system (i.e., system for handling of system management interrupts in a multiprocessor computer system; See Abstract) comprising:

- a memory (i.e., SMRAM memory space 78 in Fig. 3) with a first memory address (i.e., memory location for Operating code for SMI handler of Processor 12c in Fig. 1) having system management interrupt (SMI) code (i.e., said Operating code; See paragraphs [0005] and [0019]);
- a first processor (i.e., said Processor 12c of Fig. 1) to execute the SMI code when a SMI (i.e., SMI issued by chipset initiated by peripheral devices, e.g., keyboard, etc.) is received (in fact, said Operating code for SMI handler of Processor being executed for said initiating peripheral device; See paragraphs [0005] and [0006]); and
- a second processor (i.e., Processor 12b of Fig. 1) to execute the SMI code (See paragraph [0018], lines 13-28), if the SMI is software generated (i.e., if the SMI issued by chipset initiated by a Processor; See step 46 in Fig. 2, in fact, software SMI: See paragraph [0017], lines 21 through 27; actually, checking SMI signature in SMRAM 78 of Fig. 3).

Referring to claim 55. Nguyen teaches

- the first processor (i.e., Processor 12c in Fig. 1) has a first system management base (SMBase) address (i.e., address of SMRAM space 84 in Fig. 3).

Referring to claim 56, Nguyen teaches

- the second processor (i.e., Processor 12b in Fig. 1) has a second SMBase address (i.e., address of SMRAM space 82 in Fig. 3).

Referring to claim 57, Nguyen teaches

- the first memory address (i.e., memory location for Operating code for SMI handler of Processor 12c in Fig. 1) has an offset (i.e., a predetermined address at said memory location of said Operating code) from the first SMBase (i.e., from a starting address of SMRAM space 84 in Fig. 3; in fact, said Processor 12c is designated as default SMI handling processor, wherein said Operating code is located at said predetermined address; See paragraphs [0005], [0008], and [0019]).

Referring to claim 58, Nguyen teaches

- a target SMBase (i.e., memory location for Operating code for SMI handler of Processor 12c in Fig. 1) by default (i.e., a predetermined address at said memory location of said Operating code) is the first SMBase (i.e., address of SMRAM space 84 in Fig. 3 because said Processor 12c is designated as default SMI handling processor; See paragraph [0019]).

Referring to claim 59, Nguyen teaches

- the target SMBase is changed to the second SMBase (i.e., from SMRAM space 84 to SMRAM space 82 in Fig. 3 for Processor 12b of Fig. 1) before the second processor (i.e., said Processor

12b) executes the SMI code (See paragraphs [0018]-[0020]; in fact, a default SMI handling Processor 12c executes Operating code for SMI handler of Processor 12b in Fig. 1, which is actually the SMI code).

Referring to claim 61. Nguyen teaches

- the first and second processors (i.e., Processor 12c and Processor 12b in Fig. 1) are physical processors (See paragraph [0016], lines 1-5).

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

14. Claims 2, 17, and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dale [GB 2 382 180] as applied to claims 1, 3-5, 12-14, 18, 22, 23, 45, and 47-49 above, and further in view of Nalawadi [US 2003/0009654 A1].

Referring to claim 2. Dale discloses all the limitations of the claim 2, except that does not teach that the first and second processors are logical processors.

Nalawadi discloses a computer system having a single processor equipped to serve as multiple logical processors (See Abstract), wherein

- a physical processor (i.e., Intel® Pentium® Family Processor, e.g., Intel® Pentium® 4 Processor; See paragraph [0006], lines 1-7) serving as a first and second logical processors (i.e., multiple logical processors; See paragraph [0006], lines 7-9).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted said first and second logical processors, as disclosed by Nalawadi, for said first and second processors (i.e., GSM and MMI Processors), as disclosed by Dale, for the advantage of providing a dual-processor (i.e., multiprocessor) capability for executing multiple-tasks in parallel using a single physical processor (See Nalawadi, paragraphs [0006]-[0007]).

Referring to claims 17 and 46. Dale discloses all the limitations of the claims 17 and 46, respectively, except that does not teach that both the first and second processors are logical processors located on the same die.

Nalawadi discloses a computer system having a single processor equipped to serve as multiple logical processors (See Abstract), wherein

- both first and second processors are logical processors located on the same die
- a physical processor (i.e., Intel® Pentium® Family Processor, e.g., Intel® Pentium® 4 Processor; See paragraph [0006], lines 1-7) serving as a first and second logical processors on the same die (i.e., multiple logical processors on said Intel® Pentium® 4 Processor; See paragraph [0006], lines 7-9).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted said first and second logical processors, as disclosed by Nalawadi, for said first and second processors (i.e., GSM and MMI Sub-systems), as disclosed by Dale, for the advantage of providing a dual-processor (i.e., multiprocessor) capability for executing multiple-tasks in parallel using a single physical processor (See Nalawadi, paragraphs [0006]-[0007]).

15. Claims 6, 7, 15, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dale [GB 2 382 180] as applied to claims 1, 3-5, 12-14, 18, 22, 23, 45, and 47-49 above, and further in view of Rankin [US 5,613,071 A].

Referring to claim 6. Dale discloses all the limitations of the claim 6, except that does not expressly teach that the first memory address is aligned.

Rankin discloses a method for providing remote memory access in a massively parallel data processing system (See Abstract), wherein an atomic operation for said remote memory access comprising:

- a first memory address (i.e., said AOM Region) is aligned (See col. 14, lines 14-27).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said atomic operation, as disclosed by Rankin, in said method (i.e., a method for waking up components in a dual-processor based system), as disclosed by Dale, for the advantage of providing support for said atomic operations on remote data through said first memory address being aligned (i.e., AOM memory; See Rankin, col. 14, lines 12-13).

Referring to claim 7. Rankin teaches

- the first memory address (i.e., said AOM Region) is 4K aligned (See col. 14, lines 20-22).

Referring to claim 15. Dale discloses all the limitations of the claim 15, except that does not expressly teach that the first memory address is located in conventional memory.

Rankin discloses a method for providing remote memory access in a massively parallel data processing system (See Abstract), wherein an atomic operation for said remote memory access comprising:

- a first memory address (i.e., said AOM Region) is located in conventional memory (in fact, said AOM Region being located in Local Memory 410 starting at 0x0 in Fig. 5).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said atomic operation, as disclosed by Rankin, in said method (i.e., a method for waking up components in a dual-processor based system), as disclosed by Dale, for the advantage of providing support for atomic operations on remote data through said first memory address being located in conventional memory (i.e., AOM memory; See Rankin, col. 14, lines 12-13).

Referring to claim 16. Rankin teaches

- the first memory address (i.e., said AOM Region) is aligned (See col. 14, lines 20-22).

16. Claims 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dale [GB 2 382 180] as applied to claims 1, 3-5, 12-14, 18, 22, 23, 45, and 47-49 above, and further in view of Shimada [US 6,237,120 B1].

Referring to claim 19. Dale discloses all the limitations of the claim 19, except that does not teach that patching an instruction pointer for the second processor to a second memory address.

Shimada discloses a program patching of a ROM (See Abstract), wherein

- patching an instruction pointer (e.g., "B" in Correcting Address Register 31 and "Jump to 'L'" in Correcting Data Register 32 in Fig. 8A) for a second processor (i.e., CPU 14 of Fig. 2) to a second memory address (i.e., Address 'L' of RAM 26 in Fig. 8B).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said program patching, as disclosed by Shimada, in said method, as disclosed by Dale, for the advantage of providing an electronic apparatus in which even when a bug in the firmware is discovered after the electronic apparatus is mass-produced or even when the firmware must be modified, such problems can be solved readily easily by supplying in one step a correcting information thereto from the outside (See Shimada, col. 1, line 66 through col. 2, line 5).

Referring to claim 20. Shimada teaches

- the second memory address (i.e., Address 'L' of RAM 26 in Fig. 8B) is a non-aligned address (i.e., said Address 'L' of RAM 26 is not aligned with said Address 'B' of ROM 15 in Figs. 8A-B).

Referring to claim 21. Shimada teaches

- executing code at the second memory address (i.e., Address 'L' of RAM 26 in Fig. 8B) after patching the instruction pointer (i.e., "B" in Correcting Address Register 31 and "Jump to 'L'" in Correcting Data Register 32 in Fig. 8A) to the second memory address (See Fig. 8C; i.e., wherein executing code at Address 'L' of said RAM after patching the instruction pointer 'B' and jumping to Address 'L' of said ROM).

17. Claims 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dale [GB 2 382 180] as applied to claims 1, 3-5, 12-14, 18, 22, 23, 45, and 47-49 above, and further in view of Haren et al. [US 6,192,442 B1; hereinafter Haren].

Referring to claim 24, Dale discloses all the limitations of the claim 24, except that does not teach that an APIC is used to generate the SMI.

Haren discloses an interrupt controller (See Abstract), wherein

- an APIC (i.e., programmable interrupt controller 30 of Fig. 3; See col. 2, lines 3-11) being used to generate a SMI (i.e., SMIOUT# via pin 39 in Fig. 3; See col. 5, lines 10-20).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said APIC (i.e., programmable interrupt controller), as disclosed by Haren, in said first processor (i.e., GSM Sub-system), as disclosed by Dale, for the advantage of providing an arrangement of communicating interrupt request to said first processor (i.e., microprocessor) without consuming any of interrupt input pins (See Haren, col. 4, lines 37-40).

Referring to claim 25, Dale, as modified by Haren, teaches

- the APIC (i.e., programmable interrupt controller 30 of Fig. 3; Haren) is located in the first processor (i.e., GSM Sub-system 310 of Fig. 3; in fact, initiating signal for waking up process is generated by said GSM Sub-system, actually, GSM ULPD 314 in Fig. 3).

18. Claims 40 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dale [GB 2 382 180] in view of Nalawadi [US 2003/0009654 A1].

Referring to claim 40, Dale discloses an apparatus (i.e., cellular communication device in Fig.3) comprising:

- a controller (i.e., GSM ULPD 314 of Fig. 3) to generate a first system management interrupt (SMI; i.e., initiating signal for waking up process; See Steps 405-415 in Fig. 4, in fact, RF_Module 340 receiving RF_RADIO_ON signal 370 in Fig. 3; See page 18, lines 6-11);
- a first logical processor (i.e., GSM Processor 312 of Fig. 3), coupled to the controller (actually, said GSM Processor being coupled to said GSM ULPD in Fig. 3), to handle the first SMI (i.e.,

said waking up process) and generate a wake-up signal (in fact, said interrupt signal was caused by said RF_RADIO_ON signal from GSM Sub-system 310 in Fig. 3; See page 18, lines 27-30); and

- a second logical processor (i.e., MMI Processor 322 of Fig. 3), coupled to the controller (actually, said MMI Processor being coupled to said GSM ULPD via GPIO 321 in Fig. 3), to handle the first SMI (i.e., said waking up process) after the wake-up signal is received from the first logical processor (See page 16, line 28 through page 17, line 2).

Dale does not teach that the first and second processors are logical processors.

Nalawadi discloses a computer system having a single processor equipped to serve as multiple logical processors (See Abstract), wherein

- a physical processor (i.e., Intel® Pentium® Family Processor, e.g., Intel® Pentium® 4 Processor; See paragraph [0006], lines 1-7) serving as a first and second logical processors (i.e., multiple logical processors; See paragraph [0006], lines 7-9).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted said first and second logical processors, as disclosed by Nalawadi, for said first and second processors (i.e., GSM and MMI Processors), as disclosed by Dale, for the advantage of providing a dual-processor (i.e., multiprocessor) capability for executing multiple-tasks in parallel using a single physical processor (See Nalawadi, paragraphs [0006]-[0007]).

Referring to claim 41, Dale teaches

- the first logical processor (i.e., GSM Processor 312 of Fig. 3) executes code at a first memory location (i.e., memory element having said instructions in Memory 350 in Fig. 3) to handle the first SMI i.e., initiating signal for waking up process; See Steps 405-415 in Fig. 4, in fact, RF_Module 340 receiving RF_RADIO_ON signal 370 in Fig. 3; See page 18, lines 6-11) with

the first logical processor (See page 21, lines 9-14).

19. Claim 42 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dale [GB 2 382 180] in view of Nalawadi [US 2003/0009654 A1] as applied to claims 40 and 41 above, and further in view of Rankin [US 5,613,071 A].

Referring to claim 42. Dale, as modified by Nalawadi, discloses all the limitations of the claim 42, except that does not expressly teach that the first memory location is 1k aligned.

Rankin discloses a method for providing remote memory access in a massively parallel data processing system (See Abstract), wherein an atomic operation for said remote memory access comprising:

- a first memory address (i.e., said AOM Region) is 4k aligned (See col. 14, lines 14-27).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said atomic operation, as disclosed by Rankin, in said apparatus (i.e., cellular communication device), as disclosed by Dale, as modified by Nalawadi, for the advantage of providing support for said atomic operations on remote data through said first memory address being aligned (i.e., AOM memory; See Rankin, col. 14, lines 12-13).

Dale, as modified by Nalawadi and Rankin, does not expressly teach that said first memory location is aligned in 1k instead of 4k.

However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have set up said alignment in 1k, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art*. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

* Applicants' disclosure on page 13, paragraph [0038] states that the Applicants' invention is also picking up an optimum value from 1k, 4k, or other aligned memory address range without any particular purpose.

20. Claims 50 and 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dale [GB 2 382 180] as applied to claims 1, 3-5, 12-14, 18, 22, 23, 45, and 47-49 above, and further in view of Nguyen [US 2002/0099893 A1].

Referring to claim 50, Dale discloses all the limitations of the claim 50, except that does not teach the code at the first memory address is SMI handling code.

Nguyen discloses a system for handling of system management interrupts in a multiprocessor computer system (See Abstract), wherein

- code (i.e., Operating code for SMI handler of Processor 12c in Fig. 1) at a first memory address (i.e., memory location for said Operating code) is SMI handling code (i.e., software SMI handler; See paragraphs [0005] and [0019]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said handling of system management interrupts (i.e., software SMI handling), as disclosed by Nguyen, in said system, as disclosed by Dale, for the advantage of providing said handling of SMIs for said system (i.e., multiprocessor computer system) using only one or subset of processors (See Nguyen, paragraph [0010]).

Referring to claim 51, Dale teaches

- the wake-up signal (i.e., interrupt signal for waking up MMI Processor 322 of Fig. 3) is a vector (i.e., processor interrupt signal inherently anticipates the claimed subject matter "vector based") containing the first memory address (i.e., interruption signal generated for said MMI Processor; See page 18, line 27 through page 19, line 4).

21. Claim 60 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nguyen [US 2002/0099893 A1] as applied to claims 26-33, 35-38, 54-59, and 61 above, and further in view of Nalawadi [US 2003/0009654 A1].

Referring to claim 60. Nguyen discloses all the limitations of the claim 60, except that does not teach that the first and second processors are logical processors.

Nalawadi discloses a computer system having a single processor equipped to serve as multiple logical processors (See Abstract), wherein

- a physical processor (i.e., Intel® Pentium® Family Processor, e.g., Intel® Pentium® 4 Processor; See paragraph [0006], lines 1-7) serving as a first and second logical processors (i.e., multiple logical processors; See paragraph [0006], lines 7-9).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted said first and second logical processors, as disclosed by Nalawadi, for said first and second processors (i.e., Processors 12 in Fig. 1), as disclosed by Nguyen, for the advantage of providing a multiprocessor capability for executing multiple-tasks in parallel using a single physical processor (See Nalawadi, paragraphs [0006]-[0007]).

22. Claims 8-11 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

23. Claims 34, 43, 44, 52, and 53 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

24. Claim 39 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening

claims, and further rewritten or amended to overcome the claim objections under minor informality, set forth in this Office action.

25. The following is a statement of reasons for the indication of allowable subject matter:

With respect to claim 8, the claim limitations are deemed allowable over the prior art of record as the prior art fails to teach or suggest that handling the first SMI with the second processor comprises executing the default SMI handler located at the first memory address.

The claims 9-11 are dependent claims of the claim 8.

With respect to claim 34, the claim limitations are deemed allowable over the prior art of record as the prior art fails to teach or suggest that the second processor executes the SMI code to handle the SMI for the second processor, if the SMI is software generated.

With respect to claim 39, the claim limitations are deemed allowable over the prior art of record as the prior art fails to teach or suggest that returning the target SMBase of the SMI handler to the first SMBase after executing the SMI code to handle the SMI for the second processor.

With respect to claim 43, the claim limitations are deemed allowable over the prior art of record as the prior art fails to teach or suggest that handling the first SMI with the second logical processor comprises executing code at the first memory location.

The claim 44 is a dependent claim of the claim 43.

With respect to claim 52, the claim limitations are deemed allowable over the prior art of record as the prior art fails to teach or suggest that handling the first SMI with the second processor after receiving the wake-up signal comprising setting a pointer to a second memory address.

The claim 53 is a dependent claim of the claim 52.

Response to Arguments

26. Applicants' argument filed on 3rd of March 2006 with respect to "The Office Action requested that applicants add a 'Brief Summary of the Invention' description to the application under 37 CIRR 1.77(b). However, applicants would like to kindly point out that both the MPEP 608.01(d) and 37 C.F.R. §1.73 do not require the presence of a 'Brief Summary of the Invention.' ... It does not state 'must' or 'shall.' Accordingly, applicants have elected not to include a 'Summary of the Invention' as this is within the discretion and right of the applicants." has been fully considered but the Examiner respectfully disagrees.

In fact, Rule 37 C.F.R. §1.73 states "A brief summary of the invention indicating its nature and substance, which may include a statement of the object of the invention, **should precede** the detailed description. Such summary **should**, *when set forth*, **be** commensurate with the invention as claimed and any object recited should be that of the invention as claimed." Furthermore, Rule 37 C.F.R. §1.77(b) states "The specification **should include** the following sections in order: ..." In contrary to the Applicants' allegation, as is shown above, the Rules 37 C.F.R. §1.73 and 37 C.F.R. §1.77(b) requires "Summary of the Invention" for the current US practice in the patent application.

Moreover, the Applicants particularly stress that the Rule 37 C.F.R. §1.73 states "... summary should, ***when set forth***, be ...," and thus it is conditional (See the Response, page 13, lines 11-13). However, the term "*when...*" is not a conditional language[†] in contrary to the Applicants' assertion. Therefore, the specification requires the arrangement of "BRIEF SUMMARY OF THE INVENTION" before "BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS" in the specification on page 4, and thus, the Applicants' argument on this point is not persuasive.

[†] "when"$_{adv}$ is defined as "1: at what time; 2: a) at or during which time, b) and then; 3: at a former and usu. less prosperous time" by Merriam-Webster's Collegiate® Dictionary (10th ed.)

Conclusion

27. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Gephardt [US 5,530,891 A] discloses system management interrupt mechanism within a symmetrical multiprocessing system.

Nalawadi [US 6,968,412 B1] discloses method and apparatus for interrupt controller data re-direction.

Khouli et al. [US 6,308,278 B1] disclose supplying standby voltage to memory and wakeup circuitry to wake a computer from a low power mode.

Adjamath [US 2003/0224768 A1] discloses processor re-start control.

Yamaki [US 6,446,213 B1] discloses software-based sleep control of operating system directed power management system with minimum advanced configuration power interface (ACPI)-implementing hardware.

Hobson et al. [US 6,065,121 A] disclose control of computer system wake/sleep transitions.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 571-272-3637. The examiner can normally be reached on 9:30am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Christopher E. Lee
Patent Examiner
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CEL/

Christopher E. Lee